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10/605,110	09/09/2003	Anthony I-Chih C		Chou	FIS920030228US1	2109	
TITLE OF INVENTION: METHOD FOR SEPARATELY OPTIMIZING THIN GATE DIELECTRIC OF PMOS AND NMOS TRANSISTORS WITHIN THE SAME SEMICONDUCTOR CHIP AND DEVICE MANUFACTURED THEREBY							
APPLN. TYPE	SMALL ENTITY	SMALL ENTITY ISSUE FEE		PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE	
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KESHAVAN, BELUR V		2825		438-199000			
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